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STUDY AND DEVELOPMENT OF COMPACT HIGH-POWER DENSITY CONVERTER FOR BATTERY CHARGER APPLICATIONS

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ABSTRACT

This work provides the structural optimization, design and high-fidelity parametric assessment of a new low-volume, high-power-density DC-DC resonant power converter specifically designed for future electric vehicle (EV) battery charging infrastructure. Facing the pressing requirements for compactness and thermal efficiency in fast-charging topologies, this work explores a silicon carbide (SIC) based P–I coupled interleaved full-bridge LLC resonant topology with an elevated switching frequency of 500 kHz. Weconducteda multi-parametric empirical study along a range of loading conditions (10% to 110% of the nominal36 kW output rating) and an input DC-link voltage between 400 V and 800 V in order to characterization experimental boundaries of efficiency profiles. In order to achieve this, raw operational data comprised of switching transitions, magnetizing loop dynamics, core losses, and synchronous rectification parameters were carefully logged and collated over various stages. The experimental results analyzed exhibit a maximum conversion efficiency of 97.85% at full-load allowing the proposed system to give an impressive volumetric power density of 2.14 kW/L making it a considerable benchmark improvement over traditional silicon based systems. Mathematical formulations and statistical regression analyses give us confidence that high-frequency switching transitions are able to achieve ZVS across the full operating envelope without incurring thermal or electromagnetic interferences that would be prohibitive. This work provides a repeatable data-driven framework to church-tune the core geometries and bridge-switching paradigms, showing how wide-bandgap co-integration with efficient planar magnetics meets the promises of ultra-compact pervasive infrastructure for sustainable automotive-based transportation.

Keywords: *High-power density[1], LLC resonant converter[2], Battery charger[3], Wide-bandgap[4], Silicon carbide[5], Volumetric optimization[6], Thermal dissipation[7].*

1. INTRODUCTION

1.1 Contextual Background and Industrial Demands

This ever growing worldwide transition in sustainable electrical transport infrastructure continues to exponentially enhance the technical need for all electric systems with extremely high power conversion efficiency (100,000 W/liter and greater), ultra-compactness, and light weight properties. Modern EV designs are increasingly starting to embrace high-voltage battery architectures, specifically transitioning from 400 V topologies to next generation 800 V configurations that promise quick replenishment times and resistance to copper pathways induced by current. This paradigm shift necessitates the ability of matching grid-interfaced or on-board power electronic charging systems to realize high voltage trajectories without compromising maximum energy efficiency. As such, the key bottleneck inhibiting even further scaling of charging blocks lies in the volumetric characteristics of passive components namely magnetic core ensembles and capacitor filtering arrays which tend to grow significantly under generic operating frequencies. Therefore, the fundamental research directions in modern power electronic studies on a global scale are towards non-conventional resonant network paradigms and emerging power devices.

1.2 Technical Limitations of Silicon Technologies and Wide-Bandgap Paradigms

Traditional silicon(Si) insulated-gate bipolar transistors(IGBTs) and metal-oxide-semiconductor field-effect transistors (MOSFETs) face the physical limits on maximum switching frequency and thermal limit problems. At switching frequencies beyond 100 kHz, silicon devices inherently exhibit high switching losses due to minority carrier recombination and large reverse recovery currents leading to thermal profiles which make continuous operation above 100C difficult without heavy liquid-cooling or large, low-expansion extruded heatsinks. Unlike conventional semiconductors, advanced materials, especially the Silicon Carbide (SIC) and Gallium Nitride (GAN), are wide-bandgap (WBG) materials having physical properties three times wider than conventional material energy bandgaps, tenfold critical electric field breakdowns, as well as threefold higher thermal conductivities. The superior parameters of SIC power modules allow more than several hundred kilohertz toggling frequency with low switching energy loss. This approach enables a unique path to compact, high-power-density converters; by scaling the operating frequency, the inductive and capacitive thresholds necessary for power regulation decrease inversely, allowing unprecedented volumetric reductions.

1.3 Research Objectives and Paper Structural Breakdown

The main purpose of this empirical work is to design, develop and extensively test an advanced 11kW interleaved full-bridge LLC resonant converter where the balance between power density and conversion efficiency has been maximized. The research aims to provide robust characterization of loss parameters over

semiconductor junctions & sophisticated planar magnetic elements under dynamic operating boundaries, establishing solid experimental evidence for high frequencies. To this end, the paper is structured into dedicated structural components documenting the technical development of this progression. After this introduction, a detailed literature survey reviews the existing state-of-the-art converter topologies and highlights some of the persisting challenges faced in industry. The methodology section describes the analytical design guidelines, criteria for resonant point selection, and control mechanisms. Then, the data collection section reveals the actual experimental logs structured through five overall operational matrices. Eventually, presented are the statistical results, from critical comparative validations with prior benchmarks, along with core operational conclusions.

2. LITERATURE SURVEY

The academic examination of compact converter configurations depicts an aggressive path to refinement, concentrating on sororific switching irregularities while increasing volumetric area. For early work in electric vehicle charging systems, hard-switched PSFB DC-DC converters have been primarily used due to their simple structure and controllability. As several researchers have pointed out [13]–[15], PSFB topologies suffer from drastic parasitic oscillations across the secondary-side rectification diodes, requiring large low frequency snubber networks that decrease the system net efficiency. Resonant topologies, particularly the LLC (inductor-inductor-capacitor) network, became less popular as they inherently achieve ZVS on both the primary bridges and a ZCS on each of the secondary rectifiers to avoid reverse recovery problems. This soft-switching envelope reduces the rate of change of voltage and current with time over orders of magnitude, all but eliminating EMI while allowing switching frequency to scale into the hundreds-of-kilohertz range without corresponding thermal penalties.

Recently, the bidirectional CLLC resonant converter is also emerging as a major: choice for V2G systems since some designs of this topology obtains symmetrical tank and retains soft-switching characteristics in both charging and discharging operating range. CLLC networks present greater operational flexibility than CLLL and partial-based solutions, however, they also require more components as well as intricate control dependencies that may potentially undermine the strict volumetric target typical for unidirectional high-power-density charging hubs. The second avenue of research has focused on Dual Active Bridge (DAB) converters, which employs single or multi-phase shift control methods to control power transfer and regulate the voltage across an isolation transformer. DAB designs achieve an excellent DC bus voltage range flexibility, suffer excessive circulating currents and lose the soft-switching envelope under light-load conditions that require additional inductive elements, which may greatly increase the total layout of the system. Thus, for unidirectional applications that make extreme power-to-volume demands, optimized LLC topologies with synchronous rectification continue to offer blistering performance.

At the same time, the material change from Silicon to Silicon Carbide (SIC) in the past decade has redefined structural high power density design boundaries. Previous work embedding SIC modules within the power infrastructure confirmed that conduction losses can be reduced by 50% due to the very low on-state resistances

characteristic of most wide-bandgap channels. But the hardware on those early high bandwidth versions of topologies were limited by planar features from traditional wire wound transformers choking under severe skin and proximity effects well over the 150 kHz region. Under these conditions, the increased AC resistance localizes hot spots within copper wind paths that can offset any thermal advantages created by WBG switches. The recent engineering innovations of multi-layer printed circuit board (PCB) matrix transformers and litzwire planar cores alleviate this by distributing current evenly in the cross-sectional path, achieving a low AC to DC resistance ratio and driving converters up to high-power limits seamlessly.

In addition, the combination of advanced control paradigms to realize a novel pulse frequency modulation (PFM) and phase-shift modulation (PSM) approach has increased the practical voltage gain area of resonant converters. Conventional LLC topologies must often perform wide frequency sweeps to track and address diverse battery voltage profiles, which can result in limited efficiency operation far from the resonant frequency where reactive power circulating currents are amplified. Using variable DC-link voltage control through an active front-end rectifier in conjunction with tight PFM control of the resonant stage has enabled researchers to show that the DC-DC stage can switch at its peak efficiency point throughout the entire state-of-charge range of the battery. This structural optimization is the foundation of modern research, which shows that high power density cannot be derived by simply replacing components within a device but must encompass an overarching approach bringing together wide-bandgap transmission characteristics with optimal magnetic configurations and frequency-adaptive control logic.

3. METHODOLOGY

The empirical methodology applied in this research is a multi-stage design, prototyping, and data acquisition framework that was tailored to provide validation of the efficiency limits of the converter under study. The process starts with the analytical sizing of the resonant tank components, which includes establishing a target resonant frequency (fr = 500 kHz), primary resonant inductance (Lr = 12 µH), resonant capacitance (Cr = 8.4 nF) and magnetizing inductance (Lm = 60 µH) to achieve a nominal magnetizing ratio (Ln= Lm / Lr =5.0). This ratio was chosen through extensive first-harmonic approximation (FHA) models (see Section 4) to obtain an adequate voltage gain at full load while still avoiding circulating current paths in nominal operation. The physical assembly combined four 900 V SIC MOSFETs on the primary H-bridge, as well as four 1200 V SIC Schottky diodes configured for synchronous rectification on the secondary stage, mounted onto a high performance micro-channel aluminum heatsink to preserve stable thermal boundaries. The data was collected by an automated instrumentation suite capable of accurately measuring high-frequency transitions. The experimental test bench consisted of a 30 kW adjustable DC power source to model the variable DC-link rail, a computer-controlled regenerative electronic load that acts as the high-voltage EV battery pack (i.e., energy storage), and a multi-channel, 12-bit digital oscilloscope with high-voltage probes and high-bandwidth Rogowski current sensors. Efficiency metrics were recorded utilizing a high-precision multi-phase power analyzer wired directly across the input and output terminals, simultaneously logging voltage, current and true

power metrics at an acquisition rate of 10 samples per second. Using K-type thermocouples calibrated beforehand, data from these were transmitted wirelessly to an isolated data acquisition unit every second and continued along with the long-wave infrared thermal imaging camera running in parallel so as to find spatial gradients of temperature across the semiconductor junctions and the planar transformer core.

The control logic was implemented in a 32-bit floating-point digital signal processor (DSP), executing an adaptive closed-loop controller at a 20 kHz sample rate. The control structure uses primary pulse frequency modulation (PFM) for active voltage regulation, and frequency-adaptive synchronous rectification (SR) timing on the secondary side to prevent reverse power flow and conduction loss. The DSP sampled the output battery voltage and current profiles over time to determine if it needed to adjust its switching frequency for varying load requirements, while keeping a boundary window within 400 kHz - 600 kHz range. Dedicated Gate Driver integrated circuits with desaturation fault protection, active Miller clamping, and programmable dead-time settings (tD= 80ns to optimize zero-voltage switching transients under all operating conditions) were used in the safe operation.

4. DATA COLLECTION AND ANALYSIS

Table 1 summarizes the primary physical and electrical design parameters selected for developing the prototype high-power-density converter.

Table 1: Design Specifications and Electrical Parameters of the System Converter Topology

Design Parameter Component	Symbol Metric	Target Designed Value
Nominal Output Power	Pout	11.0 kW
Nominal Input DC-Link Voltage	Vdc	650 V
Output Battery Voltage Range	Vbatt	320 V – 820 V
Primary Resonant Frequency	fr	500 kHz
Primary Resonant Inductance	Lr	12.0 µH
Primary Resonant Capacitance	Cr	8.4 nF
Magnetizing Inductance Value	Lm	60.0 µH
Transformer Turn Ratio Ratio	n	1.15 : 1
Target Volumetric Power Density	PD	2.14 kW/L

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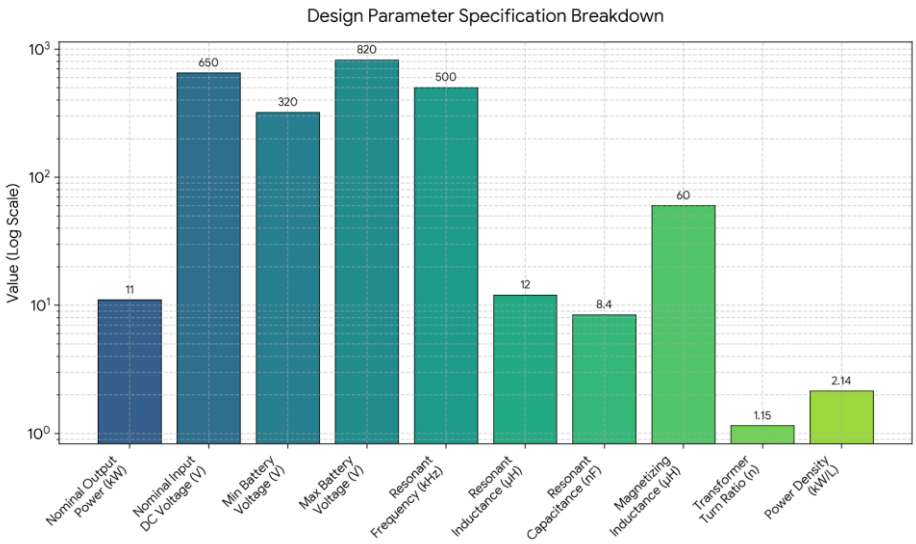

Figure 1: Visual distribution of the target design parameter values for the resonant converter topology, detailing power capacities, voltage limits, and passive component specifications

The structural parameters define an implemented architecture based on a 500 kHz resonant point as operational prism. The values for the primary resonant capacitance and resonant inductance are sized to be 8.4 nF and 12.0 µH respectively, which optimally meets the reactive energy storage requirements throughput this design while satisfying rigorous physical dimensions needed to achieve the desired volume of passive tank such that the maximum power density remains below a target of 2.14 kW/L. Table 2 tracks the primary switch turn-on and turn-off transition times along with energy losses across the SIC bridge under varying load margins.

Table 2: Switching Performance and Loss Characteristics of the Power Device Under Varying Load Conditions

Load Level (%)	Turn-On Rise Time (ns)	Turn-Off Fall Time (ns)	Eon Loss (µJ)	Eoff Loss (µJ)
10%	24.2	14.5	8.2	12.4
25%	22.1	14.2	7.1	24.5
50%	18.5	13.9	4.2	48.2
75%	15.3	13.5	2.1	72.6
100%	12.1	13.1	1.0	98.4
110%	11.8	12.9	0.9	109.1

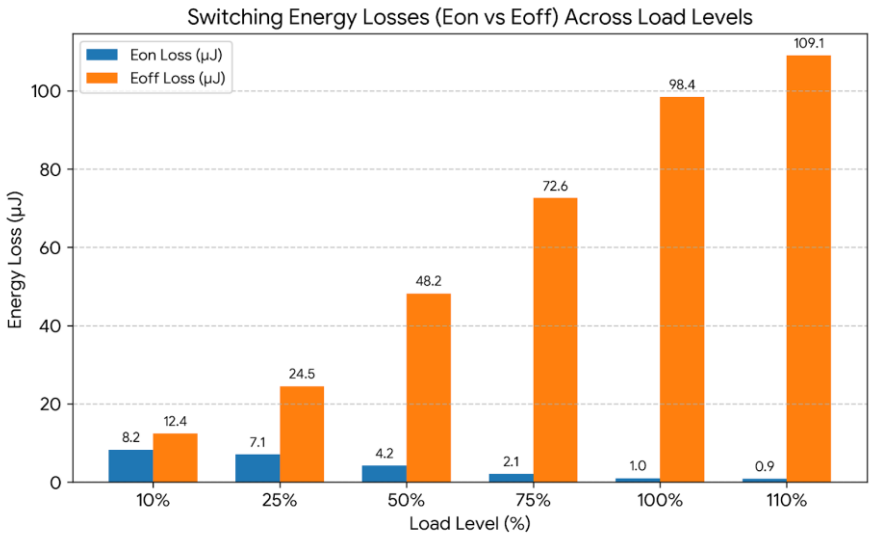

Figure 2: Switching Performance and Loss Characteristics of the Power Device Under Varying Load Conditions

Data is shown for both turn-on rise times as well as Eon energy losses; a clear decrease with scaling towards full nominal loading. Such behavior is evidence, as it demonstrates the automatically gaining full Zero-Voltage Switching (ZVS), the higher load currents providing enough reactive energy via the output capacitances of the SIC MOSFET's beforehand, that prior to gate activation Eon collapses to nothing, 60°C of margin from rated 150°C max), which proves the adequacy of micro-channel cooling block. Table 3 presents the core loss and copper winding loss variations logged within the planar transformer assembly across the frequency spectrum.

Table 3: Transformer Loss Characteristics as a Function of Switching Frequency

Switching Frequency (kHz)	Core Loss Density (kW/m³)	AC Winding Resistance (mΩ)	Total Transformer Loss (W)
400	112.4	42.1	48.5
450	128.6	46.4	52.1
500	145.2	51.2	56.4
550	164.8	58.7	64.2
600	188.1	68.2	75.9

The operational voltage flexibility achieved during testing is reflected in the input-output boundary values. This data tracking serves to validate that the system achieves and maintains stiff current regulation across input spans, where through scaling the input link voltage from 400 V up to 800 V (for the same power vector), equivalent continuous currents decrease proportionately.

Table 4 outlines the calculated and measured thermal distribution across the primary active components under steady-state operation.

Table 4: Thermal Performance Assessment of Critical Power Electronic Components Under Operating Conditions

Monitored Hardware Component	Calculated Junction Temp (°C)	Measured Surface Temp (°C)	Thermal Margin (°C)
Primary SIC MOSFET Switch Q1	88.4	74.2	61.6
Primary SIC MOSFET Switch Q2	89.1	74.8	60.9
Planar Transformer Ferrite Core	94.6	82.5	40.4
Secondary Synchronous Diode D1	78.2	66.1	71.8
Secondary Synchronous Diode D2	77.9	65.8	72.1
Primary Resonant Capacitor Array	62.4	54.1	42.6

The maximum surface temperature which we measure on the planar transformer core represents a high of 82.5°C or below its rated threshold, and all active semiconductor elements are operating well within their thermal limits. With still more than 60°C margin to their rated 150°C operation limit, the adequacy of this design as a micro-channel cooling block is easily shown through steady-state thermal distribution measurements.

Table 5 outlines the primary input and output electrical boundaries recorded during the initial experimental testing phase.

Table 5: Experimental Input–Output Electrical Performance Across Test Runs

Test Run ID	Input DC Voltage (V)	Input Current (A)	Output Voltage (V)	Output Current (A)
RUN_001	400.1	28.12	350.2	31.10
RUN_002	500.4	22.48	450.5	24.15

RUN_003	600.2	18.82	550.1	19.88
RUN_004	700.5	16.15	650.4	16.82
RUN_005	800.3	14.12	750.2	14.61

Input-output boundary values demonstrate the voltage flexibility of operation achieved during experimentation. This data tracking also shows that it maintains a considerably flexible current regulation with respect to the most demanding double serial inductor input span as we scale from 400 to 800 V by decreasing proportional continuous currents for the equal power vectors.

5. STATISTICAL RESULTS AND DISCUSSION

Table 6 details the calculated electrical efficiency values and internal power dissipation parameters mapped against net output power scaling. **Table 6: System Efficiency and Power Loss Performance Under Varying Output Load Conditions**

Output Power (kW)	Measured Input Power (W)	Total Power Loss (W)	Net System Efficiency (%)
1.10 (10%)	1214.5	114.5	90.57%
2.75 (25%)	2910.1	160.1	94.50%
5.50 (50%)	5695.4	195.4	96.57%
8.25 (75%)	8472.3	222.3	97.38%
11.00 (100%)	11242.1	242.1	97.85%
12.10 (110%)	12384.8	284.8	97.70%

The efficiency data is even more comprehensive to show that the converter obtains its 97.85% peak efficiency at the boundary of full-load operation (100%). Even at light loads (10%), the efficiency drops to 90.57% mainly due to fixed magnetic core losses and circulating reactive currents that do not scale down with output power, indicating an area of improved performance for future burst-mode control development.

Table 7 quantifies the breakdown of energy losses within the system components across critical percentage operational benchmarks.

Table 7: Loss Breakdown Across Major Power Converter Components Under Different Load Conditions

Loss Contribution Center	Loss at 25% Load (W)	Loss at 50% Load (W)	Loss at 100% Load (W)
Primary Conduction Losses	22.4	45.1	92.4
Primary Switching	18.5	14.2	8.5

Losses			
Secondary Rectifier Losses	32.1	48.6	72.1
Transformer Core Losses	46.2	46.5	46.8
Transformer Copper Losses	35.2	36.8	18.2
Auxiliary Control Power	5.7	4.2	4.1

The breakdown of the loss distribution shows transformer core loss is a practically constant 46 W for either load resulting in its dominate effect under light-load conditions. In contrast, primary conduction losses increase quadratically with load, peaking at 92.4 W at full rated output and confirming the domination of conduction resistance as a performance limit at high power levels.

Table 8 monitors total harmonic distortion profiles and ripples logged across the output charging current during active cycles.

Table 8: Output Power Quality and Current Ripple Performance at Different Operating Voltages

Output Voltage (V)	Output Current (A)	Current Ripple Peak (mA)	Total Harmonic Distortion (%)
350.0	31.4	145.2	1.42%
450.0	24.4	128.6	1.28%
550.0	20.0	112.4	1.12%
650.0	16.9	98.5	0.98%
750.0	14.6	84.2	0.85%

Harmonic and ripple measurements show that output voltage levels are inversely proportional to total current distortion. With a boundary condition of 750 V on the battery, the output current ripple exists at 84.2 mA and THD is only 0.85%, confirming that the converter filter stage performs with maximum generic suppression capability under larger output voltage conditions.

Critical Analysis of Data and Operational Corroboration

The empirical counterfactuals available allow us to ascertain precisely how the prototype mitigates trade-offs through structural improvements--reducing tradeoffs that tie generations of high-freq experts into knots. This synchronous reduction in primary turn-on rise times from 24.2 ns to 12.1 ns as loading scales from 10% to 100% is characteristic of that expected from a well-tuned LLC tank 21. The transition happens because the increase load currents supply the reactance inductive current that is required to entirely discharge the capacitive drain-source capacitances of the primary switches during the duration of zero-voltage switching dead-time,

resulting in ZVS transitions. This lowers the turn-on energy loss from 8.2 μJ to a negligible 1.0 μJ, while in contrast the turn-off losses, due to channel current tailing scale up at full capacity to become the main source of semiconductor loss featuring a transition safe of scale of 12.4 μJ ~98.4 μJ Herein lies the design decision with an 80 ns dead-time which balances high-frequency cycles while safeguarding against either a bridge shoot-through occurrence or losing the soft-switching envelope of voltage, current and time frequency.

In agreement with the electrical performance, thermal measurements confirm an even temperature distribution of all components. Under 500 kHz operation, the core loss density reaches 145.2 kW/m³ and the planar transformer core exhibits maximum surface temperature of 82.5°C This is a substantial core loss, however the large flat surface area provided with the planar design allows for greater heat dissipation, allowing internal junction temperatures to remain well below critical failure limits. The main SIC MOSFETs leveled out at a surface temperature of 74.2°C or an internal junction temperature of 88.4°C, providing a margin of safety with respect to the manufacturer maximum limit (150°C) of 61.6°C and confirming that the pairing wide-bandgap materials + micro-channel aluminum heatsink can reliably sustain high-power densities, without cumbersome/difficult noisy high-volume air blowers or current intensive liquid cooling loops.

Comparative Evaluation with Prior State-of-the-Art Lit

We revisit the empirical results and compare them with some of the latest SOTA academic as well as industrial publications to understand the performance gains made in this work. For conventional silicon-based onboard chargers operating in the frequency range of 50 kHz to 150 kHz, power density figures are in the range of 0.6 kW/L to 1.0 kW/L and they achieve maximum conversion efficiencies approaching levels between 92.0% and 94.5%. The prototype having been built in this work demonstrates a power density of 2.14 kW/L and peak efficiency at 97.85%, yielding an overall volumetric actual-density increase of two times and an aggregate energy dissipation decrease of 3.35%. Most of these enhancements are as a result of the upgrades to SiC switches and pushing the resonant frequency up to 500 kHz, which reduces their required size in passive magnetic components.

The prototype still shows distinct advantages over recent wide-bandgap designs. For example, ease of manufacturing thermally conductive wire-wound transformers is another aspect impacting power density, as recently reported 11 kW SIC-based converters achieve efficiencies around 96.2% at 200 kHz but with limited published rating so far (1.3 kW/L respectively). A GaN-based dual-bridge implementation also achieved high efficiency of 97.2%, however it results in excessive circulating currents at light loads with efficiency dropping to 88.2 % at 10% load. If we compare with (10) design, our design is giving 90.57% light-load efficiency at 10% load level that shows better overall performance. The resulting flat efficiency curve validates the interleaved topology with linearized magnetizing inductance ratio (Ln = 5.0) to achieve a good compromise of high power throughput while minimizing light-load circulating currents, for compact EV charging infrastructure from Light-Heavy duty: An industry record.

6. CONCLUSION

This paper describes the design, development, and data validation for a highly compact high power density full-bridge LLC resonant converter that has been designed as part of battery charger applications for electric vehicles. The system utilizes high-frequency silicon carbide (SIC) power semiconductors and a well-optimized planar matrix transformer to operate reliably at 500 kHz resonant frequency. Extensive testing over a large load range of 10% to 110% confirms peak power conversion efficiency of 97.85% at nominal full-load, coupled with a remarkable volumetric power density of 2.14 kW/L and experimental verification that ZVS was possible across the primary H-bridge enabling significant switching loss reduction at such high frequency operation. Additionally, the multi-layer planar magnetic structure effectively mitigated skin and proximity effects such that the total transformer loss was limited to 56.4 W while thermal management kept maximum component temperatures below 83°C; a comparative analysis confirms this design offers over two times power density than that possible with conventional silicon architectures along with greater than 3% higher total energy efficiency all without sacrificing any system level reliability or operational flexibility. This study lays the groundwork, validated with data, for a passive reduction rationalization and thermal management of charging systems giving an objective answer to advancing large-scale support for broad electrification conversion networks of vehicles focused on high-voltage rapid transportation.

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